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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/977,699 | 10/16/2001 | Thomas N. Indermaur | 10007795-1 | 3755 |

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| EXAMINER | |
|---|---|
| DIMYAN, MAGID Y | |
| ART UNIT | PAPER NUMBER |
| 2825 | |

DATE MAILED: 02/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/977,699 | Applicant(s) INDERMAUR, THOMAS N. | |
|---|---|---|---|
| | Examiner Magid Y Dimyan | Art Unit 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to because they include the following informality: in Fig. 3a, the GND1 inputs to the ten latches shown should be changed to GND, in order to comply with the specification. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baisuck et al (U.S. Patent No 5,299,139) in view of McSherry et al (U.S. Patent No. 6.230,299). Baisuck et al (hereafter, Baisuck) disclose a short-circuit locator method that uses an improved circuit layout verifying system (see Abstract and column 2, lines 34 – 43 as

well as other portions of the disclosure). However, Baisuck does not teach running a connectivity extract tool on the artwork (layout), or comparing the artwork (layout) of the circuit to the schematic (Layout versus Schematic – or LVS comparison). However, McSherry et al (hereafter McSherry) recite a method and apparatus for extracting and storing connectivity and geometrical data for an IC design that uses a connectivity extract tool (see Abstract) and running LVS for layout verification (see column 4, line 65 and column 5, line 17). Since it would be advantageous to be able to check for short circuits in a complex Integrated circuit design expeditiously, it would therefore be obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Baisuck and McSherry to achieve the same invention as claimed.

4. Claims 2, 3, 4, 5, 6, 7, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baisuck in view of McSherry and further in view of Heile et al (U.S. Patent No. 6,321,369). As per claims 2, 5 and 6, the teachings of Baisuck and McSherry are cited above and in their disclosures. However they do not teach creating a copy of their artwork (layout) and inferring labels to that copy. Heile, et al (hereafter, Heile) on the other hand disclose an electronic design methodology that makes use of copying, deleting, renaming, adding, as well as other editing choices (see column 13, line 40) with their analysis tools. The analysis tool includes a layout editor (see column 8, line 35) so that changes (like adding/deleting labels) can be made. See also column 7, line 36 and column 8, lines 20 – 25 for a layout versus schematic check – claim 6. As per

claim 3, see Baisuck (column 13, lines 3 – 4) that teaches the use of text files in the analysis of circuit shorts. As per claim 4, see Baisuck (column 4, lines 53 – 56) that recites locating erroneous connections in a circuit (i.e., each component). Referring to claims 6 – 9, Heile teaches how to create a base design output file and one or more variation output design files (see Abstract). The designer can then modify the variation output files, run the connectivity extract tool, LVS, etc on the copy. Since creating a copy of the layout, using additional labels on the copy, and the use of connectivity text files would facilitate the debugging process for locating shorts in an IC design (which includes electrical connections of all the components), it would therefore be obvious to one having ordinary skill in the art at the time the invention was made to combine all three disclosures to obtain the same inventions as claimed herein.

5. Claims 10, 11, 12, 13, 14, 15, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bartels et al (U.S. Patent No. 6,275,974) in view of Heile. Referring to claims 10, 13 and 14, Bartels et al (hereafter, Bartels) recites a method for tracing (i.e., determining) a short in a VLSI circuit as a shortest path using the layout of the design, i.e. artwork (see Abstract and Background of the Invention). However, they do not teach creating a copy of the artwork, and inferring labels to the copy of the artwork. As recited above, Heile discloses these inventions. Claims 10 – 17 are therefore rejected for the same reasons given in paragraph 4 above for rejecting claims 2 – 9, respectively. Since creating a copy of the layout, using additional labels on the copy, and the use of connectivity text files would facilitate the debugging process for

locating the shortest path for a short in an IC design (which includes electrical connections of all the components), it would therefore be obvious to one having ordinary skill in the art at the time the invention was made to combine the two disclosures to obtain the same inventions as claimed.

## *Conclusion*

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,178,539 to Papadopoulou et al teaches a method for computing critical are for shorts of a layout using Voronoi diagrams.

U.S. Patent No. 6,507,932 to Landry et al discloses a method of converting or translating a layout or schematic netlist to a simulation netlist comprising the steps of identifying net-shorted elements in the layout or schematic netlists.

Pub. No. US 2002/0046386 to Skoll et al recites a design analysis workstation for performing design analysis for ICs and provides facilities for extracting design and layout information from digital image-mosaics.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y Dimyan whose telephone number is (703) 308-1354. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Magid Y Dimyan
Examiner
Art Unit 2825

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January 30, 2003

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800